CLAIMS

Having thus described my invention, what I claim as new and desire to secure by Letters Patent is:

1. A bipolar transistor comprising:

a substrate,

an insulating layer over said substrate,

a first single crystal semiconductor layer positioned over said insulating layer having a lightly doped region of a first type and at least one contiguous heavily doped region of said first type, said lightly doped region and said contiguous heavily doped region functioning as a collector,

a second patterned semiconductor layer of a second type formed over said lightly doped region of said first semiconductor layer to function as the base, and

a third patterned semiconductor layer of said first type positioned over said second semiconductor layer to function as the emitter,

said lightly doped region of said first type having a dopant concentration to fully deplete of mobile charge through said first semiconductor layer to said insulating layer.

2. A bipolar transistor of claim 1 wherein said first single crystal semiconductor layer has a thickness in the range from 30 to 1000 nanometers.

3. A bipolar transistor comprising:

a substrate,

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an insulating layer over said substrate,

a first single crystal semiconductor layer positioned over said insulating layer having a lightly doped region of a first type and at least one contiguous heavily doped region of said first type, said lightly doped region and said contiguous heavily doped region functioning as a collector, a top region of said lightly doped region is counter-doped to a second type to function as the base,

a second patterned semiconductor layer of said second type formed over a region of said counter-doped region of said first semiconductor layer to function as the extrinsic base, and

a third patterned semiconductor layer of said first type positioned over said counter-doped region of said first semiconductor layer to function as the emitter,

said lightly doped region of said first type having a dopant concentration to fully deplete of mobile charge through said first semiconductor layer to said insulating layer.

4 A bipolar transistor of claim 3 wherein said first single crystal semiconductor layer has a thickness in the range from 80 to 1050 nanometers.

5. A bipolar transistor of claim 1 wherein said second patterned semiconductor layer is a silicon-germanium alloy.

6. An integrated-circuit chip containing

first kind of bipolar transistors of claim 1 wherein said first type doped regions are n type and said second type doped regions are p type,

and second kind of bipolar transistors of claim 1 wherein said first type doped regions are p type and said second type doped regions are n type,

said substrate of said first kind of bipolar transistors and said substrate of said second kind of bipolar transistors are the same, and

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said insulating layer over said substrate of said first kind of bipolar transistors and said insulating layer over said substrate of said second kind of bipolar transistors are the same.

7. An integrated-circuit chip containing

first kind of bipolar transistors of claim 3 wherein said first type doped regions are n type and said second type doped regions are p type,

and second kind of bipolar transistors of claim 3 wherein said first type doped regions are p type and said second type doped regions are n type,

said substrate of said first kind of bipolar transistors and said substrate of said second kind of bipolar transistors are the same, and

said insulating layer over said substrate of said first kind of bipolar transistors and said insulating layer over said substrate of said second kind of bipolar transistors are the same.

8. An integrated-circuit chip containing

bipolar transistors of claim 1, and

p-channel MOSFETs and n-channel MOSFETs wherein the source and drain regions of said MOSFETs extend downward to said insulating layer over said substrate of said bipolar transistors.

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9. An integrated-circuit chip containing

bipolar transistors of claim 3, and

p-channel MOSFETs and n-channel MOSFETs wherein the source and drain regions of said MOSFETs extend downward to said insulating layer over said substrate of said bipolar transistors.

10. An integrated-circuit chip containing

bipolar transistors of claim 5, and

p-channel MOSFETs and n-channel MOSFETs wherein the source and drain regions of said MOSFETs extend downward to said insulating layer over said substrate of said bipolar transistors.

11. An integrated-circuit chip containing

first kind of bipolar transistors of claim 1 wherein

said first type doped regions are n type and said second type doped regions are p type,

and second kind of bipolar transistors of claim 1 wherein said first type doped regions are p type and said second type doped regions are n type,

said substrate of said first kind of bipolar transistors and said substrate of said second kind of bipolar transistors are the same,

a2 said insulating layer over said substrate of said first kind of bipolar transistors and said insulating layer over said substrate of said second kind of bipolar transistors are the same, and

p-channel MOSFETs and n-channel MOSFETs wherein the source and drain regions of said MOSFETs extend downward to said insulating layer over said substrate of said bipolar transistors.

12. An integrated-circuit chip containing

first kind of bipolar transistors of claim 3 wherein said first type doped regions are n type and said second type doped regions are p type,

and second kind of bipolar transistors of claim 3 wherein said first type doped regions are p type and said second type doped regions are n type,

said substrate of said first kind of bipolar transistors and said substrate of said second kind of bipolar transistors are the same,

said insulating layer over said substrate of said first kind of bipolar transistors and said insulating layer over said substrate of said second kind of bipolar transistors are the same, and

p-channel MOSFETs and n-channel MOSFETs wherein the source and drain regions of said MOSFETs extend downward to said insulating layer over said substrate of said bipolar transistors.

13. A method for forming a bipolar transistor comprising the steps of

Selecting a substrate having an insulating layer over said substrate and

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A first single crystal semiconductor layer positioned over said insulating layer, forming lightly doped region of a first type and at least one contiguous heavily doped region of said first type in said first semiconductor layer, said lightly doped region and said contiguous heavily doped region functioning as a collector,

forming and patterning a second patterned semiconductor layer of a second type formed over said lightly doped region of said first semiconductor layer to function as the base, and

forming and patterning a third patterned semiconductor layer of said first type positioned over said second semiconductor layer to function as the emitter,

said lightly doped region of said first type having a dopant concentration to fully deplete of mobile charge through said first semiconductor layer to said insulating layer.

14. A method for forming a bipolar transistor comprising the steps of:

Selecting a substrate having

an insulating layer over said substrate and

a first single crystal semiconductor layer positioned over said insulating layer, forming a lightly doped region of a first type and at least one contiguous heavily doped region of said first type in said first semiconductor layer, said lightly doped region and said contiguous heavily doped region functioning as a collector, a top region of said lightly doped region includes the step of counter-doping to a second type to function as the base,

forming and patterning a second patterned semiconductor layer of said second type formed over a region of said counter-doped region of said first semiconductor layer to function as the extrinsic base, and

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forming and patterning a third patterned semiconductor layer of said first type positioned over said counter-doped region of said first semiconductor layer to function as the emitter,

said lightly doped region of said first type having a dopant concentration to fully deplete of mobile charge through said first semiconductor layer to said insulating layer.

15. A bipolar transistor of claim 13 wherein said second patterned semiconductor layer includes the step of forming a silicon-germanium alloy.

16. A method of forming an integrated-circuit chip comprising the steps of:

forming a first kind of bipolar transistors of claim 1 wherein said first type doped regions are n type and said second type doped regions are p type, and

forming a second kind of bipolar transistors of claim 1 wherein said first type doped regions are p type and said second type doped regions are n type,

said substrate of said first kind of bipolar transistors and said substrate of said second kind of bipolar transistors are the same, and

said insulating layer over said substrate of said first kind of bipolar transistors and said insulating layer over said substrate of said second kind of bipolar transistors are the same.

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17. A method of forming an integrated-circuit chip comprising the steps of:

forming a first kind of bipolar transistors of claim 3 wherein said first type doped regions are n type and said second type doped regions are p type, and

forming a second kind of bipolar transistors of claim 3 wherein said first type doped regions are p type and said second type doped regions are n type,

said substrate of said first kind of bipolar transistors and said substrate of said second kind of bipolar transistors are the same, and

said insulating layer over said substrate of said first kind of bipolar transistors and said insulating layer over said substrate of said second kind of bipolar transistors are the same.

18. A method of forming an integrated-circuit chip comprising the steps of:

forming bipolar transistors of claim 1, and

forming p-channel MOSFETs and n-channel MOSFETs wherein the source and drain regions of said MOSFETs extend downward to said insulating layer over said substrate of said bipolar transistors.

19. A method of forming an integrated-circuit chip comprising the steps of:

forming bipolar transistors of claim 3, and

forming p-channel MOSFETs and n-channel MOSFETs wherein the source and drain regions of said MOSFETs extend downward to said insulating layer over said substrate of said bipolar transistors.

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20. A method of forming an integrated-circuit chip comprising the steps of:

forming a bipolar transistors of claim 5, and

forming a p-channel MOSFETs and n-channel MOSFETs wherein the source and drain regions of said MOSFETs extend downward to said insulating layer over said substrate of said bipolar transistors.

21. A method of forming an integrated-circuit chip comprising the steps of:

forming a first kind of bipolar transistors of claim 1 wherein said first type doped regions are n type and said second type doped regions are p type,

forming a second kind of bipolar transistors of claim 1 wherein said first type doped regions are p type and said second type doped regions are n type,

said substrate of said first kind of bipolar transistors and said substrate of said second kind of bipolar transistors are the same,

said insulating layer over said substrate of said first kind of bipolar transistors and said insulating layer over said substrate of said second kind of bipolar transistors are the same, and

forming p-channel MOSFETs and n-channel MOSFETs wherein the source and drain regions of said MOSFETs extend downward to said insulating layer over said substrate of said bipolar transistors.

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22. A method of forming an integrated-circuit chip comprising the steps of:

forming a first kind of bipolar transistors of claim 3 wherein said first type doped regions are n type and said second type doped regions are p type,

forming a second kind of bipolar transistors of claim 3 wherein said first type doped regions are p type and said second type doped regions are n type,

said substrate of said first kind of bipolar transistors and said substrate of said second kind of bipolar transistors are the same,

said insulating layer over said substrate of said first kind of bipolar transistors and said insulating layer over said substrate of said second kind of bipolar transistors are the same, and

forming p-channel MOSFETs and n-channel MOSFETs wherein the source and drain regions of said MOSFETs extend downward to said insulating layer over said substrate of said bipolar transistors.